Claims:

1. An integrated circuit chip, comprising:

a) core logic;

b) an on-chip JTAG TAP coupled to said core logic;

c) an on-chip JTAG master coupled to said JTAG TAP; and

d) an on-chip microprocessor interface coupled to said JTAG master.

2. The chip according to claim 1, further comprising:

e) a plurality of registers coupled to said microprocessor interface and to said JTAG master.

3. The chip according to claim 2, wherein:

said plurality of registers includes a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register.

4. The chip according to claim 3, wherein:

said plurality of registers includes a start bit register and an end bit register.

5. The chip according to claim 1, wherein:

said chip has more than five pins and five of said pins are coupled to said on-chip JTAG TAP forming a JTAG interface to said chip.

6. The chip according to claim 5, further comprising:

e) switching means for selectively decoupling said JTAG interface from said JTAG TAP.

7. The chip according to claim 6, wherein:

said switching means is coupled to and controllable by said JTAG master.

8. The chip according to claim 7, wherein:

said switching means couples said JTAG master to said JTAG TAP when said JTAG interface is decoupled from said JTAG TAP, and

said switching means couples said JTAG interface to said JTAG TAP when said JTAG master is decoupled from said JTAG TAP.

9. An integrated circuit chip, comprising:

a) core logic;

b) an on-chip JTAG TAP coupled to said core logic;

c) an on-chip JTAG interface selectively coupled to said JTAG TAP;

d) an on-chip microprocessor interface selectively coupled to said JTAG TAP; and

e) switching means for selectively coupling said JTAG interface and said microprocessor interface to said JTAG TAP.

10. The chip according to claim 9, wherein:

said switching means operates to decouple said JTAG interface from said JTAG TAP when said microprocessor interface is coupled to said JTAG TAP, and

said switching means operates to decouple said microprocessor interface from said JTAG TAP when said JTAG interface is coupled to said JTAG TAP.

11. The chip according to claim 9, wherein:

said microprocessor interface includes a plurality of registers.

12. The chip according to claim 9, wherein:

said switching means is controllable via said microprocessor interface.

13. The chip according to claim 12, further comprising:

f) a switching means enable interface for receiving a signal to enable said switching means, wherein

said switching means is inoperable without receiving said signal.

14. The chip according to claim 13, wherein:

in the absence of said signal said switching means decouples said microprocessor interface from said JTAG TAP and couples said JTAG interface to said JTAG TAP.

15. The chip according to claim 11, wherein:

said plurality of registers includes a TDI FIFO, a TMS FIFO, a TDO FIFO, and a counter register.

16. The chip according to claim 15, wherein:

said TDI FIFO and said TMS FIFO each being N-bits in size, and

said microprocessor interface includes means for performing TAP operations having bit counts in excess of N-bits.

17. The chip according to claim 16, wherein:

means for performing TAP operations having bit counts in excess of N-bits includes means for cycling said TAP through state elements and holding it in one of four states.

18. The chip according to claim 17, wherein:

said four states include Test-logic Reset, Run-Test Idle, Pause-IR, and Pause-DR.

19. An integrated circuit chip, comprising:

a) core logic;

b) an on-chip JTAG TAP coupled to said core logic;

c) an on-chip JTAG master selectively coupled to said JTAG TAP;

d) an on-chip JTAG interface selectively coupled to said JTAG TAP; and

e) switching means for selectively coupling said JTAG master and said JTAG interface to said JTAG TAP.

20. The chip according to claim 19, wherein:

said switching means operates to decouple said JTAG interface from said JTAG TAP when said JTAG master is coupled to said JTAG TAP, and

said switching means operates to decouple said JTAG master from said JTAG TAP when said JTAG interface is coupled to said JTAG TAP.